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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,003	09/11/2003	Young-Bae Jung	21C-0085	5938

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EXAMINER	
CHEN, WEN YING PATTY	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,003	JUNG ET AL.	
	Examiner	Art Unit	
	Wen-Ying P. Chen	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24,26,27,30 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24,26,27,30 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on Dec. 23, 2005 has been entered.

Response to Amendment

Applicant's Amendment filed Dec. 23, 2005 has been received and entered. Claims 1-24, 26-27 and 30-31 remain pending in the current application.

Allowable Subject Matter

The indicated allowability of claims 1-22 is withdrawn in view of the newly discovered reference(s) to Takahashi et al. [A] (US 2003/0063080), Takahashi et al. [B] (US 2003/0112382), Ishige et al. (US 2004/0012744) and Tsuyuki et al. (US 6853361). Rejections based on the newly cited reference(s) follow.

The indicated allowability of claims 26-27 is withdrawn in view of the newly discovered reference(s) to Takahashi et al. [A] (US 2003/0063080), Takahashi et al. [B] (US 2003/0112382) and Ishige et al. (US 2004/0012744). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "wherein the semiconductor layer corresponds to the first connecting lines" in claims 8 and 19 is a relative term which renders the claim indefinite. The term " wherein the semiconductor layer corresponds to the first connecting lines " is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It is not clearly defined as to how the semiconductor layer corresponds to the first connecting lines. For the purpose of examination, claims 8 and 19 will be interpreted as meaning wherein the semiconductor layer is formed in the peripheral region underlying the second connecting lines as shown in Figure 4 of the Drawings acting as another insulating layer between the first and second connecting lines.

Claim Rejections - 35 USC § 103

Claims 1-2, 4-7, 9-10, 12-13, 15-18 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. [A] (US 2003/0063080) in view of Takahashi et al. [B] (US 2003/0112382).

With respect to claims 1 and 12 (Amended): Takahashi et al. [A] disclose in Figure 1 a liquid crystal display device comprising: a liquid crystal display panel including a first substrate, a second substrate facing the first substrate, and a liquid crystal layer disposed between the first and second substrates (Paragraphs 0003-0005), the first substrate including a display region and a peripheral region (as shown in Figure 1) adjacent to the display region, the display region having a plurality of pixels (Paragraph 0043), a plurality of data lines (element DL) and a plurality of scan lines (element GL), the peripheral region having a first peripheral region (element SUB1) adjacent to first ends of the data lines and a second peripheral region adjacent to first ends of the scan lines (as shown in Figure 1, region where the data lines do not cross the gate lines);

a driver section including a scan driver circuit (element GDR1) and a data driver circuit (element DDR), the scan driver circuit and the data driver circuit formed in the first peripheral region, the scan driver circuit providing the scan lines with a scan driving signal, and the data driver circuit providing the data lines with a data signal; and

a first connecting part, formed in the second peripheral region to be coupled to the first ends of the scan lines, the first connecting part including a plurality of groups, the scan driving signal being applied to the first connecting part.

Takahashi et al. [A] fail to disclose that each of the groups of the first connecting part is disposed in layers different from each other.

However, Takahashi et al. [B] disclose in Figure 8 groups of connecting scan lines (element GIL), which are disposed in layers different from each other.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a liquid crystal display device as taught by Takahashi et al. [A] wherein the groups of connecting scan lines are disposed in layers different from each other as taught by Takahashi et al. [B], since Takahashi et al. [B] teach that by forming the scan lines in adjacent to each other in different layers allows wide spacing between the adjoining signal lines in the same layer to greatly reduce shorting troubles between the signal lines (Paragraphs 0175-0176).

As to claims 2 and 13: Takahashi et al. [B] further disclose in Figures 11A-11D that the first connecting part includes: a first group having a plurality of first connecting lines (element GIL) formed from a same layer as the scan lines (element GL); and a second group having a plurality of second connecting lines (element GIL) formed from a same layer as the data lines (element DL).

As to claims 4 and 15: Takahashi et al. [B] further disclose in Figure 8 that the substrate further comprises a first insulating layer (element GI), interposed between the first and second connecting lines, for electrically insulating the first connecting lines from the second connecting lines.

As to claims 5 and 16: Takahashi et al. [B] further disclose in Figure 11A that the pixels respectively include a switching device coupled to one of the data lines and one of the scan lines, the switching device has a control electrode (element GL), a first current electrode (element SD2), a second current electrode (element SD1), a second insulating layer (element GI), a semiconductor layer (element AS), a second insulating layer formed on the control electrode, the semiconductor layer formed on the second insulating layer, the first and second current

electrodes formed on the semiconductor layer to be separated from each other by a predetermined distance.

As to claims 6 and 17: Takahashi et al. [B] further disclose in Figures 11A-11D that the first insulating layer (element GI) is a same layer as the second insulating layer (element GI).

As to claims 7 and 18: Takahashi et al. [B] further disclose in Figures 11A-11D that the first insulating layer (elements GI and AS combined) includes the second insulating layer (element GI) and the semiconductor layer (element AS).

As to claims 9 and 20: Although not shown in the figures of Takahashi et al. [B], it is obvious that a contact hole is formed in the first insulation layer for exposing the first ends of the scan lines so that the first connecting lines are electrically connected to the first ends of the scan lines through the contact hole (0174-0176).

As to claims 10 and 21 (Amended): Takahashi et al. [A] further disclose in Figure 1 that the substrate further includes a second connecting part (lines connected to element GDR2), the second connecting part is formed in a third peripheral region (as shown in the figure), is coupled to second ends of the scan lines (element GL) and includes a plurality of third groups of connecting lines, the region is adjacent to the second ends of the scan lines, the scan driving signal is applied to the second connecting part.

Takahashi et al. [A] fail to disclose that each of the groups of the second connecting part is disposed in layers different from each other.

However, Takahashi et al. [B] disclose in Figure 8 groups of connecting scan lines (element GIL), which are disposed in layers different from each other.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a liquid crystal display device as taught by Takahashi et al. [A] wherein the groups of connecting scan lines are disposed in layers different from each other as taught by Takahashi et al. [B], since Takahashi et al. [B] teach that by forming the scan lines in adjacent to each other in different layers allows wide spacing between the adjoining signal lines in the same layer to greatly reduce shorting troubles between the signal lines (Paragraphs 0175-0176).

Claims 3, 8, 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. [A] (US 2003/0063080) and Takahashi et al. [B] (US 2003/0112382) in view of Ishige et al. (US 2004/0012744).

With respect to claims 3 and 14: Takahashi et al. [A] and Takahashi et al. [B] disclose all of the limitations set forth in the previous claims, but both fail to specifically disclose that the first connecting lines partly overlaps with at least one of the second connecting lines.

However, Ishige et al. disclose in Figures 3 and 5 of stacking scan lines wherein the first group of connecting lines (element GC5) completely overlaps the second connecting lines (element GC1) or that the second connecting lines are formed between the first connecting lines so as to reduce the influence of waveform rounding and noise on image quality (Paragraph 0072).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a liquid crystal display device as taught by Takahashi et al. [A] and Takahashi et al. [B] wherein the first connecting lines partly overlaps the second connecting

lines as taught by Ishige et al., since Ishige et al. teach that by forming the first and second connecting lines in stacked form the peripheral area of the display can be made narrower so that the actual display area can be made larger and also the width of each of the connecting lines can be made thick as to prevent disconnection, further, by not completely overlapping the two groups of connecting lines allows the interference between the lines to be reduced (Paragraphs 0066-0072).

As to claims 8 and 19: Takahashi et al. [A] and Takahashi et al. [B] disclose all of the limitations set forth in the previous claims, but both fail to specifically disclose that the semiconductor layer corresponds to the first connecting lines.

However, Ishige et al. disclose in Figure 5 wherein the semiconductor layer (element 3) corresponds to the first connecting lines (element GC5), meaning wherein the semiconductor layer is formed in the peripheral region underlying the second connecting lines (element GC1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a liquid crystal display device as taught by Takahashi et al. [A] and Takahashi et al. [B] wherein the semiconductor layer corresponds to the first connecting lines as taught by Ishige et al., since Ishige et al. teach that by forming the semiconductor layer between the first connecting lines and the second connecting lines further helps to insulate the first and second connecting lines from each other in addition to the insulating layer (Paragraph 0077).

Claims 11 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. [A] (US 2003/0063080) and Takahashi et al. [B] (US 2003/0112382) in view of Tsuyuki et al. (US 6853361).

Takahashi et al. [A] and Takahashi et al. [B] disclose all of the limitations set forth in the previous claims, but both fail to disclose that the first connecting part is electrically coupled to odd numbered scan lines, and the second connecting part is electrically coupled to even numbered scan lines.

However, Tsuyuki et al. disclose in Figure 5 a substrate wherein the first connecting part (element G1) is electrically coupled to odd number scan lines, and the second connecting part (element G2) is electrically coupled to even number scan lines (Abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a liquid crystal display device as taught by Takahashi et al. [A] and Takahashi et al. [B] wherein the first connecting part is electrically coupled to odd numbered scan lines, and the second connecting part is electrically coupled to even numbered scan lines as taught by Tsuyuki et al., since Tsuyuki et al. teach that such configuration of the scan lines helps maintain wire reliability while the wiring spacing is narrowed, thus the wiring area occupying in the panel is decreased (Column 2, lines 33-46).

Claims 23-24, 26-27 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. [A] (US 2003/0063080) in view of Takahashi et al. [B] (US 2003/0112382) further in view of Ishige et al. (US 2004/0012744).

With respect to claims 23-24 and 30-31 (Amended): Takahashi et al. [A] disclose in Figure 1 a liquid crystal display device and the method of making the same comprising:

forming a first substrate including a display region and a peripheral region (as shown in Figure 1) adjacent to the display region, the display region having a plurality of pixels (Paragraph 0043), a plurality of data lines (element DL) and a plurality of scan lines (element GL), and a plurality of pixels, each of the pixels having a switching device electrically coupled to one of the scan lines and one of the data lines and a second substrate facing the first substrate, and a liquid crystal layer disposed between the first and second substrates (Paragraphs 0003-0005).

Takahashi et al. [A] further disclose that the peripheral region having a first peripheral region (element SUB1) adjacent to first ends of the data lines and a second peripheral region adjacent to first ends of the scan lines (as shown in Figure 1, region where the data lines do not cross the gate lines);

a driver section including a scan driver circuit (element GDR1) and a data driver circuit (element DDR), the scan driver circuit and the data driver circuit formed in the first peripheral region, the scan driver circuit providing the scan lines with a scan driving signal, and the data driver circuit providing the data lines with a data signal; and

a first connecting part, formed in the second peripheral region to be coupled to the first ends of the scan lines, the first connecting part including a plurality of groups, the scan driving signal being applied to the first connecting part.

Takahashi et al. [A] fail to disclose that the specific steps of forming the active substrate wherein each of the groups of the first connecting part is disposed in layers different from each

other and that the first connecting lines partly overlaps with at least one of the second connecting lines.

However, Takahashi et al. [B] disclose in Figures 11A-11D the method of forming the active substrate, wherein a first metal layer in the display region and the peripheral region is formed and patterned to form the scan lines (element GIL) and gate electrodes (element GL) branched from the scan lines on the display region and to form a plurality of first connecting lines in the peripheral region so that the first connection lines are electrically and directly coupled to a first group of the scan lines;

an insulation layer (element GI), an active layer (element AS) and a contact layer (element d0) is formed on the first substrate on which the scan lines, the gate electrodes, and the first connecting lines are formed and the active layer and the contact layer are patterned to form an active pattern and a contact pattern;

a second metal layer is formed on the insulation layer, the active pattern, and the contact pattern, which are then patterned to form the data lines (element DL), source electrodes (element SD2) branched from the data lines, drain electrodes (element SD1) spaced apart from the source electrode on the display region and second connecting lines (element GIL) that are electrically and directly coupled to a second group of the scan lines, wherein the first connecting lines are formed from a same layer as the scan lines and the second connecting lines are formed from a same layer as the data lines.

Ishige et al. disclose in Figures 3 and 5 of stacking scan lines wherein the first group of connecting lines (element GC5) completely overlaps the second connecting lines (element GC1)

or that the second connecting lines are formed between the first connecting lines so as to reduce the influence of waveform rounding and noise on image quality (Paragraph 0072).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a liquid crystal display device as taught by Takahashi et al. [A] wherein the groups of connecting scan lines are disposed in layers different from each other as taught by Takahashi et al. [B], since Takahashi et al. [B] teach that by forming the scan lines in adjacent to each other in different layers allows wide spacing between the adjoining signal lines in the same layer to greatly reduce shorting troubles between the signal lines (Paragraphs 0175-0176) and wherein the first connecting lines partly overlaps the second connecting lines as taught by Ishige et al., since Ishige et al. teach that by forming the first and second connecting lines in stacked form the peripheral area of the display can be made narrower so that the actual display area can be made larger and also the width of each of the connecting lines can be made thick as to prevent disconnection, further, by not completely overlapping the two groups of connecting lines allows the interference between the lines to be reduced (Paragraphs 0066-0072).

As to claim 26: Ishige et al. further disclose in Figures 3 and 5 that a double insulation layer (elements 2 and 3 combined) on the peripheral region is formed interposed between the insulation layer and the second connecting lines.

As to claim 27: Ishige et al. further disclose in Paragraphs 0068-0070 that the different layered gate connection lines are electrically connect to the each of the gate lines, therefore, it is obvious that contact holes are formed so as to expose the scan lines for electrically connecting the gate connection lines to the gate lines.

Response to Arguments

Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wen-Ying P. Chen whose telephone number is (571)272-8444. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wen-Ying P Chen
Examiner
Art Unit 2871

WPC
2/10/06

ANDREW SCHECHTER
PRIMARY EXAMINER